REMARKS

At the outset, the Examiner is thanked for the review and consideration of the present application. Claims 1-20 are now pending in the application. Claims 1, 4-12, and 18-20 have been amended. The basis for the amended claims may be found throughout the specification, drawings, and claims of the original application. The Examiner is respectfully requested to reconsider and withdraw the rejection(s) in view of the amendments and remarks contained herein.

Claim Rejections –35 USC § 103

Claims 1-8, 17-18 and 20 are rejected under 35 USC 103(a) as being unpatentable over Ikegami et al. (US 2003/0160339) in view of Kurita et al. (US 6,399,891). Applicant respectfully traverses the rejection at least for the reasons set forth below:

Applicant respectfully submits that claim 1 is not obvious over Ikegami in view of Kurita. Claim 1 is currently amended to clearly present that the resin-copper coating includes a resin layer and a copper layer thereon, a gap is formed to expose a portion of the resin layer between two sections of the second layer, and an electronic component is connected to the two sections of the topmost circuit layer adjacent to the gap so as to at least partially cover the exposed portion of the resin layer.

For example, as shown in FIG. 8 of the present invention, the electronic component 30a is disposed across the gap on the second circuit layer 22 by soldering tin balls 32. In other words, the electronic component 30a bridges on the gap connecting to different sections of the second circuit layer 22. In another example, the electronic component 30b is embedded in the gap and bonded with silver-filled epoxy (silver paste) to the resin layer 15, and multiple wires 31 are bonded around the electronic component 30b to electrically connect the second electronic component 30b to different sections of the second circuit layer 22. In other words, the electronic component 30b is disposed on the exposed portion of the resin layer within the gap. More particularly, the present invention provides a method for preparing thin integrated circuits including the step of connecting an electronic component to two sections of the topmost (second) circuit layer

adjacent to a gap so as to at least partially cover the exposed portion of the resin layer.

Applicant submits that these features are not disclosed in Ikegami in view of Kurita. Ikegami disclosed an electronic element 9 fixed onto a first conductive film 7 is electrically connected to a second conductive film 8, as shown in FIG. 2B. That is, the electronic element 9 is entirely disposed on the conductive film 7. The electronic element 9 of Ikegami is neither disposed across the gap on the two films 7and 8, nor within the gap between the two films 7 and 8.

Kurita disclosed a multiplayer board 1 includes alternating polyimide films 11-16 and copper films 21-26. However, Kurita fails to disclose an electronic component is connected to the two sections of the topmost circuit layer adjacent to the gap so as to at least partially cover the exposed portion of the resin layer.

Applicant respectfully submits that both Ikegami and Kurita fail to disclose an electronic component is connected to the two sections of the topmost circuit layer adjacent to the gap so as to at least partially cover the exposed portion of the resin layer. Accordingly, Applicant submits that claims1-8, 17-18 and 20 are nonobvious over this combination of references and should be patentable.

Claims 9-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikegami in view of Kurita and further in view of Farnworth (US 6,365,501).

The Examiner cites the Farnworth reference to show solder balls formed of lead and tin used to join a chip to a carrier such as a printed wiring board. Applicant submits that, even if the Farnworth reference does teach these features, it does not aid the Ikegami and Kurita references to overcome its deficiencies as noted above. Accordingly, Applicant submits that claims 9-12 define over this combination of references as well.

Claims 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikegami in view of Kurita and further in view of Lin et al. (US 5,200,362), Carey et al. (US 5,672260), and Meyrat et al. (US 4,842,536)

The Examiner cites the Lin reference to show the substrate being removed and an isolating layer being applied to the exposed first circuit layer and the Meyrat reference to show a tin paste soldering material arranged on a printed circuit board.

Applicant submits that, even if the Lin and Meyrat references do teach these features, it does not aid the Ikegami and Kurita references to overcome their deficiencies as noted above. Accordingly, Applicant submits that claims 13-16 are nonobvious over this combination of references as well.

Claims 13-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikegami in view of Kurita and further in view of Whetsel (US 2002/0021140).

The Examiner cites the Whetsel reference to show that smaller transistor may be embedded within integrated circuits to enable the development of smaller, lower power electronic consumer products. However, Whetsel only disclosed more and more functional circuitry may be embedded in integrated circuits fabricated on a wafer (See FIG. 1A). Applicant respectfully submits that Whetsel fails to elaborate how a transistor is integrated within integrated circuits. In general, a transistor is sequentially formed with integrated circuit design, instead of being inserted or disposed onto a predefined area of a resin layer above a circuit layer, which will then become a connecting layer to other circuit boards. More particularly, Whetsel fails to disclose the step of connecting an electronic component to two sections of the topmost (second) circuit layer adjacent to a gap so as to at least partially cover the exposed portion of the resin layer. Even if the Whetsel reference does teach a transistor may be embedded within integrated circuits fabricated on a wafer, there is still no teaching, motivation, suggestion, or incentive to combine the Whetsel reference with Ikegami in view of Kurita to overcome its deficiencies as noted above. Accordingly, Applicant submits that claims 13-16 are patentable over this combination of references as well.

Furthermore, claims 2-17 depend from claim 1, and as such, are also considered to be allowable. In addition, each of these claims recites other features which make these claims additionally allowable.

Regarding claim 18, Applicant respectfully submits that claim 18 is not obvious over Ikegami in view of Kurita. Claim 18 currently amended to clearly present that an electronic component is disposed within the gap and connects to two sections of the topmost circuit layer adjacent to the gap. For the reasons stated above, Applicant submits that these features are not disclosed in Ikegami in view of Kurita. Accordingly, Applicant submits that claim 18 is nonobvious over this combination of references and

should be patentable. Furthermore, claim 19 depends from claim 18, and as such, is also considered to be allowable.

Regarding claim 20, Applicant respectfully submits that claim 20 is not obvious over Ikegami in view of Kurita. Claim 20 is currently amended to clearly present that an electronic component is disposed across the gap on two sections of the topmost circuit layer. For the reasons stated above, Applicant submits that these features are not disclosed in Ikegami in view of Kurita. Accordingly, Applicant submits that claim 20 is nonobvious over this combination of references and should be patentable.

Conclusion

In view of the amendments set forth above, Applicant respectfully submits that all pending claims 1-20 are in condition for allowance, and respectfully requests the reconsideration and withdrawal of the rejections. Accordingly, a Notice of Allowance is respectfully requested.

Respectfully submitted,

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